IN THE CLAIMS

1-10. (Cancelled)

11. (Currently Amended) An I/O interface circuit comprising:

a clock generation circuit generating a first clock signal;

a jitter generator generating jitter in the first clock signal based on a setting signal, which sets a present condition of the jitter;

a data transmission ~~circuit~~ circuitry transmitting data in sync with the first clock signal including the jitter;

a data reception ~~circuit~~ circuitry receiving the transmitted data,

wherein the clock generation circuit also supplies a second clock signal to the data reception ~~circuit~~ circuitry;

wherein the data transmission ~~circuit~~ circuitry comprises:

a pattern generation circuit generating a data pattern for a jitter resistance test, and

a transmission circuitry ~~circuit~~ allowing the data pattern generated by the pattern generation circuit to be transmitted in sync with the first clock signal, and

wherein the data reception ~~circuit~~ circuitry comprises:

a reception circuitry allowing the data pattern transmitted by the transmission ~~circuit~~ circuitry to be received in sync with the second clock signal, and

a pattern comparison circuit comparing the data pattern received by the reception circuitry ~~circuit~~ with an expectation value to output a comparison result, and

a jitter generator control circuit controlling the jitter generator to vary an amount of modulation or the frequency of the jitter in accordance with the comparison result delivered by the pattern comparison ~~circuit~~ circuitry and a measurement procedure for the jitter resistance test.

12. (Previously Presented) The I/O interface circuit according to claim 11, wherein the jitter generator control circuit controls the jitter generator so as to vary the amount of modulation of the jitter when the comparison result delivered by the pattern comparison circuit indicates a match and to vary the frequency of the jitter when the comparison result delivered by the pattern comparison circuit indicates a mismatch.

13. (Currently Amended) An I/O interface circuit comprising:

a clock generation circuit generating a first clock signal;

a jitter generator generating jitter in the first clock signal based on a setting signal, which sets a present condition of the jitter;

a data transmission circuit transmitting data in sync with the first clock signal including the jitter; and

a data reception circuit receiving the transmitted data,

wherein the clock generation circuit also supplies a second clock signal to the data reception circuit;

wherein the data transmission circuit comprises:

a pattern generation circuit generating a data pattern for a jitter resistance test, and

a transmission ~~circuit~~ circuitry allowing the data pattern generated by the pattern generation circuit to be transmitted in sync with the first clock signal,

wherein the data reception circuit comprises:

a reception ~~circuit~~ circuitry allowing the data pattern transmitted by the transmission circuit to be received in sync with the second clock signal, and

a pattern comparison circuit comparing the data pattern received by the reception ~~circuit~~ circuitry with an expectation value to output a comparison result, and

wherein

the pattern generation circuit in the data transmission circuit comprises:

a circuit including data of a contiguous sequence of 0s or 1s in the data pattern, and

the pattern comparison circuit in the data reception circuit comprises

a first circuit detecting the data of the contiguous sequence of 0s or 1s having been received, and

a second circuit forcing the comparison result to indicate a match when the first circuit detects the data of the contiguous sequence of 0s or 1s having been received.

14. (Previously Presented) The I/O interface circuit according to claim 13, wherein

the pattern generation circuit in the data transmission circuit replaces part of the data pattern with the data of a the contiguous sequence of 0s or 1s, thereby allowing the data pattern to include the data of the contiguous sequence of 0s or 1s.

15. (Previously Presented) The I/O interface circuit according to claim 13, wherein the pattern generation circuit in the data transmission circuit inserts the data of the contiguous sequence of 0s or 1s into a midpoint of the data pattern, thereby allowing the data pattern to include the data of the contiguous sequence of 0s or 1s.

16. (Previously Presented) The I/O interface circuit according to claim 13, wherein the pattern generation circuit in the data transmission circuit further comprises a circuit adjusting a cycle in a case of the data of the contiguous sequence of 0s or 1s being included in the data pattern in that cycle.

17. (Cancelled)

18. (Withdrawn) A data transmission device comprising:

a clock generation circuit generating a clock signal;

a jitter generator generating jitter in the clock signal based on a setting signal, which sets a present condition of the jitter; and

a data transmission circuit transmitting data in sync with the clock signal including the jitter;

a first voltage controlled oscillator receiving the clock signal including the jitter; and

a second voltage controlled oscillator receiving a signal from the jitter generator.

19. (Cancelled)

20. (Withdrawn) An I/O interface circuit comprising:

a clock generation circuit generating a first clock signal;

a jitter generator generating jitter in the first clock signal based on a setting signal, which sets a present condition of the jitter;

a data transmission circuit transmitting data in sync with the first clock signal including the jitter;

a first voltage controlled oscillator receiving the first clock signal including the jitter; and

a second voltage controlled oscillator receiving a signal from the jitter generator.

21. (Canceled)